TOPS: An Architectural Simulation Tool for Modern PLL Design

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***Abstract*—We present a versatile simulation tool, TOPS[1], for the design, analysis, and verification of phase-locked loops. After reviewing the key design challenges for modern PLL architectures, we describe the extensive functionality of TOPS that allows the circuit designer to rapidly and thoroughly explore the PLL design parameter space for a variety of complex PLL architectures, including digital PLLs, fractional-N PLLs, and spread-spectrum PLLs. TOPS drastically reduces the development time of these circuit specifications. Preliminary results obtained from an early version of the TOPS program are presented, showing significant improvements in performance via using TOPS as compared to industry-standard simulators in use today. The paper also briefly describes the architecture of TOPS and its versatility, which allows the user to easily reconfigure the various components of the PLL as well as account for nonlinearities in them. Finally, the paper presents some of the planned future directions of this simulation tool.**

I. Introduction

Phase-locked loops (PLLs) are analog/mixed-signal circuits widely used as clock generators, frequency synthesizers or in clock/data recovery in a variety of semiconductor chips. Increasingly, system designs expect improved performance while demanding stricter tolerances. With demands of shorter turnaround times, the need for a streamlined PLL design process has become increasingly evident. Traditionally, simulation of a PLL design has been the bottleneck in the entire process taking hours and even days for exhaustive testing.

As noted previously by many researchers [6][1], the simulation of PLLs is challenging primarily due to the fact that while clock signal frequencies at various points in the PLL are usually high (MHz - GHz), the overall loop dynamics are relatively lower by a few orders of magnitude. Traditional fixed-time-step simulation tools must, therefore, perform fine-grained simulations of the entire system to obtain the behavioral characteristics of the PLL. This results in a significant cost in time and energy. Seasoned designers have relied on their experience as well as linearized models to design PLL loop parameters to match required criteria. Testing has usually involved simulation of the individual components of the PLLs while exhaustive closed-loop performance testing is done on silicon.

Researchers in academia and industry have come up with numerous solutions to the aforementioned problems. In [6], the researchers propose a discrete time domain uniform step simulator for fast simulation of PLL circuits. Authors in [1] present a polynomial interpolation system to detect switching events. However, the paper does not address time-varying systems like fractional-N PLLs. In [5], the authors introduce a novel technique to deal with non-idealities in the PLL loop by introducing a non linear model for the VCO. However, they still assume a linear model for the loop filter. In [2], the authors propose SIMPLL, an event driven PLL simulator. However, fractional-N PLLs and time-varying properties of the loop filter are ignored.

Further, despite these advances, there seems to be a lack of true parameter exploration and architecture analysis PLL simulation tools targeted to aid the circuit designer in the design of modern PLL circuits. The sheer number of choices for individual components and its architecture, the process of designing a PLL to meet certain specifications remains an art perfected through trial and error methods albeit following some basic guidelines.

The purpose of this paper is to introduce a new mathematically and circuit accurate variable step behavioral simulation tool, TOPS, that eases the design process for a wide variety of commonly used modern PLL architectures while providing the flexibility to allow for very specific tests and conditions. The tool provides a simple User Interface with a powerful simulation engine that improves the simulation speed in comparison to other standard simulation techniques. It allows the incorporation of nonlinear circuit characteristics into all PLL components as well as the capability to study time varying loop characteristics. The paper is organized as follows: Sections II and III describe the implementation details and functionality of TOPS. Sections IV and V describe case studies where the tool was used to design and fine tune architecture of PLL to meet required specifications. Section VI contains some concluding remarks along with proposed improvements and features.

II. Implementation of PLL Sub-Blocks in TOPS

A typical PLL has the following functional components as shown in Fig. 1. More detailed description of the operation of the PLL can be found in [2].

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[1] Third-Order -Plus PLL Architecture Simulator (TOPS) ; www.ghzcircuits.com/TOPS

While the fundamental principles of operation of PLLs are well known, the implementation of its components and the synthesis of signals significantly affect their behavior. Inevitably, one or more of the components in the PLL have nonlinear characteristics. This, along with the presence of widely varying frequency ranges within the closed loop, and the fact that the system could be time varying in the case of fractional-N designs, makes the study and design of PLLs challenging.

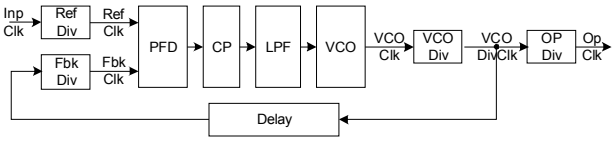

Figure 1 Diagram of PLL showing the various functional blocks

The primary intention of TOPS, in its current form, is to provide PLL designers with a tool that is versatile enough to allow "quick and accurate" check of an initial PLL design as well as perform a thorough behavioral analysis of a mature PLL design ready for on chip testing. While the simulation results produced by TOPS are accurate, it is not intended to replace final transistor level simulations performed before fabrication, but to substantially improve development time to reach that stage.

The implementations of the basic building blocks of the proposed simulation tool are as below.

1) Phase Frequency Detector (PFD)

In TOPS, a basic behavioral model of this component is used and it can be modeled as one of many standard linear or bang-bang phase or phase/frequency detectors. Options to include a dead zone, or conversely, a region of higher gain at small phase errors are also available.

2) Charge Pump (CP)

In TOPS, the authors ignore the slew-rate effects on the charge pump current, but allow users to specify the magnitude of the current pulse as a function of the error pulse width. The magnitude of each of the currents can be modeled independently and as nonlinear.

3) Low-pass Loop Filter (LPF)

Currently, TOPS allows users to choose between second order and third order passive filters, each with an option of simulating in the presence of capacitor leakage currents. Each of the filter components and the magnitude of leakage currents could be modeled as nonlinear. The leakage currents could also be modeled as time-varying to emulate noise or other modulating factors.

4) Voltage Controlled Oscillator (VCO)

The VCO is usually characterized by two quantities: the nominal frequency, f_{nom}, and the VCO gain, K_{vco}. As the output frequency is usually a nonlinear function of the control voltage, TOPS simulator allows user to specify these quantities with the option of specifying the nonlinear properties of the VCO.

5) Frequency Dividers

In TOPS, dividers are modeled to be simple programmable counter circuits whose ratio may change from one cycle to another (fractional-N PLLs).

6) Clock Signals

The various clock signals associated with the PLL are shown in Fig. 1. All TOPS clock signals are saved for each simulation run for detailed analysis if necessary. They are modeled as time-period arrays which can be (a) created by TOPS, (b) calculated as a result of the simulation, or (c) created by the user using any standard text editor. They can also be stored for use as input signals in future tests.

III. TOPS FUNCTIONALITY

TOPS has a comprehensive suite of analyses built-in that allows designers to quickly and easily validate a selected PLL architecture and arrive at design parameters to meet architectural specifications with just a few clicks of a button. At the same time, it is versatile enough to allow the designer to easily configure the tool and set up detailed application specific tests using a variety of input signals and accurate nonlinear component models to thoroughly test a given design. Fig. 2 shows the tabbed feature of the tool with drop down menus where the user can specify the necessary components of the different functional blocks of the PLL described in Section II, specify other parameters like minimum accuracy and the format of output data files and specify specific tests and analyses to be performed.

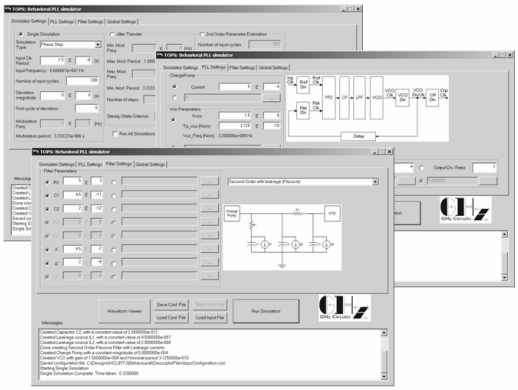

Fig. 2 User Interface to specify component parameters/models, analyses and other settings

The various tests and analyses currently available in TOPS are briefly described in the following subsections.

1) Single Simulations

The user can run quick single simulations such as phase/frequency step response, single tone frequency modulation response or user defined reference input response to analyze impulse/step responses, acquisition and noise response with linear and non-linear components and under static/time-varying conditions. The user can also define the input clock as any jittery pseudo-random data stream to analyze performance of clock/data

recovery loops.

2) Jitter Transfer Characteristics

This test provides the user a push button analysis of the frequency response of the closed loop system to phase modulated input, in order to determine the jitter transfer characteristics. TOPS reports the peak jitter transfer as well as the -3dB gain frequency, and outputs the frequency response data in both time and frequency domain.

3) Open loop frequency response (Bode Plot)

This test provides the user a push button analysis of the frequency response of the open loop system to determine stability margins. TOPS reports the unity gain frequency and the phase margin of the system, and outputs the frequency response data in both time and frequency domain.

4) Parameter Estimation (2^{nd} Order Approximation)

Often, higher order PLLs are approximated as second order systems to define natural frequency (ω_n) and damping factor (ζ). User specified step input is applied and best-fit ζ and ω_n of the equivalent second order approximation are estimated based on the step response.

IV. CASE STUDY I: DESIGN OF SPREAD SPECTURM FRACTIONAL-N PLL FOR A CONSUMER APPLICATION

The application of TOPS in the design of a spread spectrum PLL with specifications shown in Table I is now described.

Table I: PLL Design Specifications for case study

Parameter	Value
Fin	4MHz
Fout	80MHz
Spread Spectrum Range	Programmable ±5%, ±3.5%, ±1.5%, ±0.75%
Spread Spectrum Frequency	Between 10 & 20 KHz
Current Consumption	< 1mA
PLL phase margin	> 45°
Technology	0.13u

The most striking specification is the low power consumption. Meeting this stringent requirement requires architectural tradeoffs and low power circuit implementation techniques. On first inspection, three possible choices for architectures become apparent, namely (a) Integer-N PLL with analog modulation, (b) Integer-N PLL with digital post-processing for spread-spectrum (c) Fractional-N PLL with ΣΔ-type modulation. Choice (a) was rejected as control of spread spectrum ranges over PVT is not straightforward. Choice (b) was rejected as digital implementations of spreading the spectrum will very likely not meet the current consumption budget.

It was decided to implement solution (c) with the variable divider controlled by hard-wired ΣΔ modulator (implemented as a ROM sequence generator) as shown in Fig. 3.

The key design challenge was to arrive at the parameters of the loop filter which resulted in closed loop BW just low enough to filter out the 1 bit modulated divider control into an acceptable triangular ramp in frequency with acceptable ripple, while still achieving 45° phase margin. This is where the speed advantage of the tool becomes apparent. While a traditional SPICE-level circuit simulation for a time period of 300uS took 2 days, even with relaxed accuracy settings, the same simulation in TOPS completed within 5 seconds with good accuracy, thereby enabling iterative solution for the filter values.

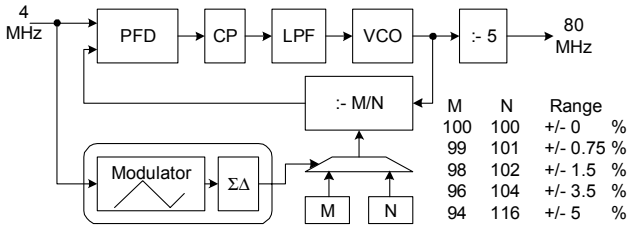

Fig. 3 Block Diagram for Spread Spectrum PLL

The sequence generator is driven off the reference clock and outputs a sequence of 1's and 0's over a 256 bit cycle. A higher density of 0's represents net lower frequency and vice-versa. This results in a binary frequency modulation sequence with a modulation frequency of 15.625KHz. The PLL has to be designed filter out the 1-bit modulation into a triangular waveform.

The VCO is required to operate up to 420 MHz and a conventional ring oscillator based design was used which resulted in KVCO at 400MHz ranging from 0.8 – 1.2GHz/V over PVT with worst case current consumption of 0.3mA.

To minimize the area of the LPF, the CP current was chosen to be nominal 3uA. A passive 2^{nd} order LPF was used. Through iterative runs of TOPS, the final filter values were selected to be 400pf, 40pf, 20KΩ.

Acquisition and steady state response of the PLL was analyzed using the Frequency Step Response feature. Fig. 4 shows the instantaneous VCO frequency vs. time illustrating both, the acquisition of the PLL with the spread spectrum modulation (variable divider) turned on, as well as the steady state operation. The total CPU time for the simulation was 3.4 s.

The closed loop jitter transfer characteristics for the PLL operating at nominal VCO frequency of 400MHz was analyzed using the Jitter Transfer Characteristics feature. A transient simulation for 10 logarithmically spaced points (*i.e.*, phase modulated reference clock) in the range of 10KHz to 300KHz resulted in closed loop 3dB bandwidth measurement as 133MHz with jitter peak of 1.89dB. Total CPU time for the simulation was 29.9 s.

The open loop Bode plot characteristics for the PLL operating at nominal VCO frequency of 400MHz was analyzed using the Bode plot feature. An open loop transient simulation for the same number of frequency points as for the jitter transfer analysis resulted in phase margin measurement as 50.3°. Total CPU time for the simulation was 37.9 s.

Using the first-cut design parameters for the PLL, circuits were built and sub-circuit parameters for each sub-circuit, *i.e.*, K_{VCO}, I_{CP}, R_Z, C_1, C_2 were extracted for a large sample space

of PVT variations. Using TOPS, the full loop PLL characteristics were obtained over this PVT space and after an iteration of re-tweaking the circuits, the sub-circuits were finalized to meet specifications as shown in Table I. The PLL is currently being laid out prior to fabrication.

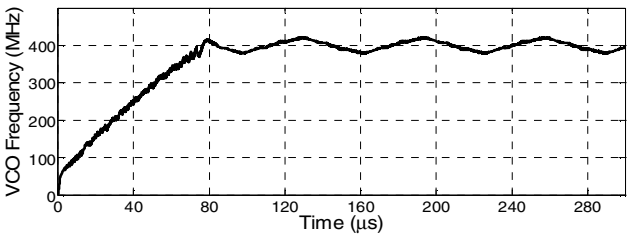

Fig. 4. Instantaneous VCO frequency; acquisition to steady state response.

V. Case Study II: Analysis of PLL Loop Filter Leakage for 10 Gigabit Ethernet Application

The application of TOPS in the analysis of impact of capacitor leakage on deterministic jitter is now described.

As designs migrate towards lower geometries, the transistors become leakier. In standard CMOS flows, the highest density of capacitance is offered by the gate oxide of the smallest geometry devices, *i.e.*, transistors with minimum T_{ox}. Thus, area considerations make it desirable to use these devices as on-chip loop filter elements. However, the devices being leaky, will contribute towards increased deterministic jitter. TOPS can be used to quickly determine how these physical phenomena impact the PLL jitter performance.

By architectural analysis, the following nominal parameters were determined as optimal for the PLL: F_{IN}=66.67MHz, F_{VCO}=3.2GHz, F_{OUT}=800MHz, K_{VCO}=150MHz/V, I_{CP}=0.5mA, R_Z=5KΩ, C_1=45pF, C_2=2pF. It is required that deterministic jitter be less than 1ps rms.

All other circuit non-idealities being ignored, leakage discharges the capacitors (being referenced to ground) and the loop has to inject charge every cycle to maintain phase lock. This causes a static phase error (SPE) at the inputs and a ripple in V_{ctrl}, which causes jitter. Steady state SPE and RMS jitter were analyzed using the Single Simulation feature. Each simulation for 10,000 VCO cycles took 0.36 seconds. Table II lists the SPE and RMS Jitter as a function of leakage current for the PLL described above. RMS period jitter is calculated as defined in [4].

Table II: SPE and RMS Jitter as function of capacitor gate leakage

Leakage Current µA/pF	Static Phase Error pS	RMS Jitter pS
0.01	14.1	0.058
0.1	141	0.57
1.0	1410	5.08

Fig. 5 shows the loop response to a slow transient ramp of leakage current, which goes from 0 to 45µA in 15µs, *i.e.* 48000 VCO cycles. The total CPU time for simulation was 1.25s.

In that particular 90nm technology, gate leakage of core devices connected as capacitor could exceed 1µA/pF. Usage of these devices as capacitors will cause unacceptable deterministic jitter. Therefore the decision was made to use thick oxide devices as capacitors, at the cost of area.

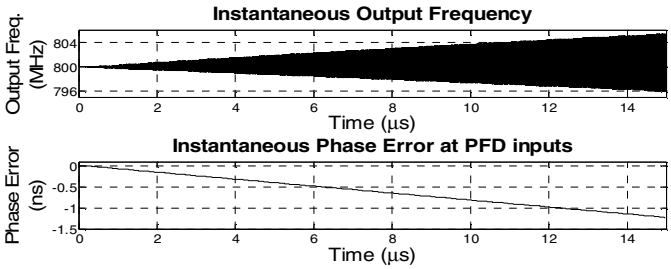

Fig. 5. Response to a slow transient ramp in leakage current.

VI. Conclusion

This paper presents ongoing efforts to create a fast design tool to design PLL circuits from design specifications as well as test PLL designs thoroughly and accurately. Care is being taken to provide maximum flexibility by allowing the user to define a variety of nonlinear circuit characteristics of the components along with the capability to simulate the system with a variety of inputs. It provides the user the ability to run fractional-N simulations as well as investigate acquisition characteristics with relative ease. Efforts are underway to expand the number of user selectable topologies for the PLL sub-blocks, incorporate random noise modeling, frequency domain analysis of PLL outputs and optimization features such as arriving at sub-circuit parameters from loop performance specifications.

Acknowledgement

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References

[1] A. Demir, E. Liu, A. L.Sangiovanni-Vincentelli, I. Vassiliou, "Behavioral simulation techniques for phase/delay-locked systems," *IEEE Custom Integrated Circuits Conference*, pp. 453-456, May 1994.

[2] F.M. Gardner, *Phaslock Techniques* 3rd Edition, John Wiley & Sons, 2005.

[3] C. D. Hedayat, A. Hachem, Y. Leduc, G. Benbassat, "Modeling and Characterization of the 3rd Order Charge-Pump PLL: a Fully Event-driven Approach*," Analog Integrated Circuits and Signal Processing*, vol. 19(1), pp. 24 – 45, April 1999.

[4] IEEE Draft P802.3an/D4.0, pp. 137, 2006

[5] X. Lai, Y. Wan, J. Roychowdhury, "Fast PLL simulation using nonlinear VCO macromodels for accurate prediction of jitter and cycle-slipping due to loop non-idealities and supply noise," *Proc. of the 2005 conference on Asia South Pacific design automation*, pp. 459-464, 2005.

[6] M.H. Perrott, "Fast and Accurate Behavioral Simulation of fractional-N Frequency Synthesizers and other PLL/DLL Circuits," *Design Automation Conference*, June, 2002, pp. 498 - 503.

[7] B. D. Smedt, G. Gielen, "Models for Systematic Design and Verification of Frequency Synthesizers," *IEEE Trans. On Circuits and Systems II.*, vol. 46(10), pp. 1301 – 1308, Oct.1999.

[8] J. Zou, D. Mueller, H. Graeb, U. Schlichtmann, E. Hennig, R. Sommer, "Fast Automatic Sizing of a Charge Pump Phase-Locked Loop based on Behavioral models," *IEEE International Behavioral Modeling and Simulation Workshop.* pp. 100 – 105, Sept. 2005.